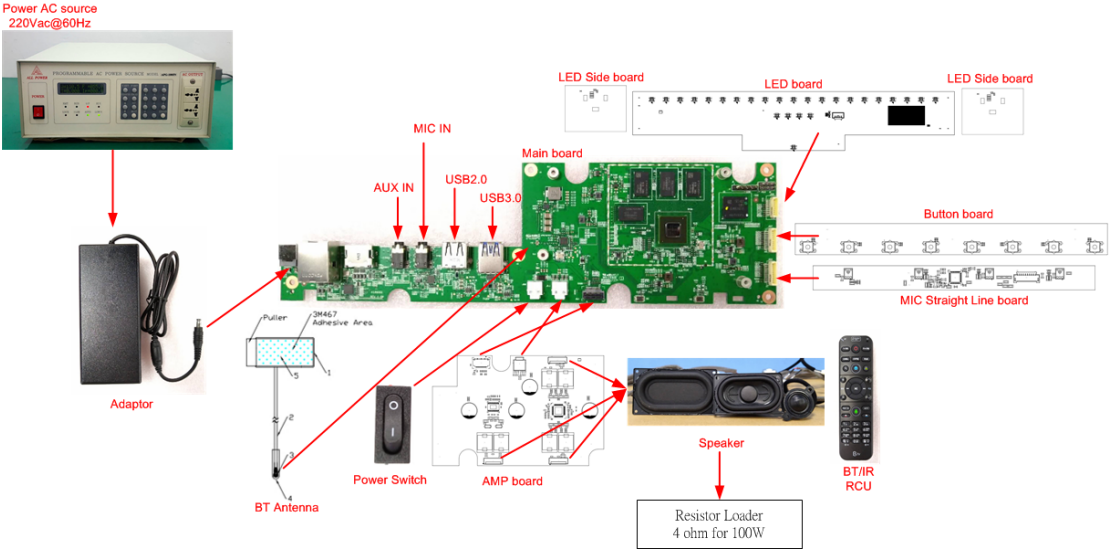


Hardware Unit Test Report

DC Power Sequence Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
V015	k000a-r52101c_EMC_ND_fac-20200928	S/N: YUHOY13-2154002298-01S1N	DDR: 1. K4A8G165WC-BCTD 2. K4A4G165WF-BCTD eMMC: KLM8G1GETF-B041

1. Power Test Setup



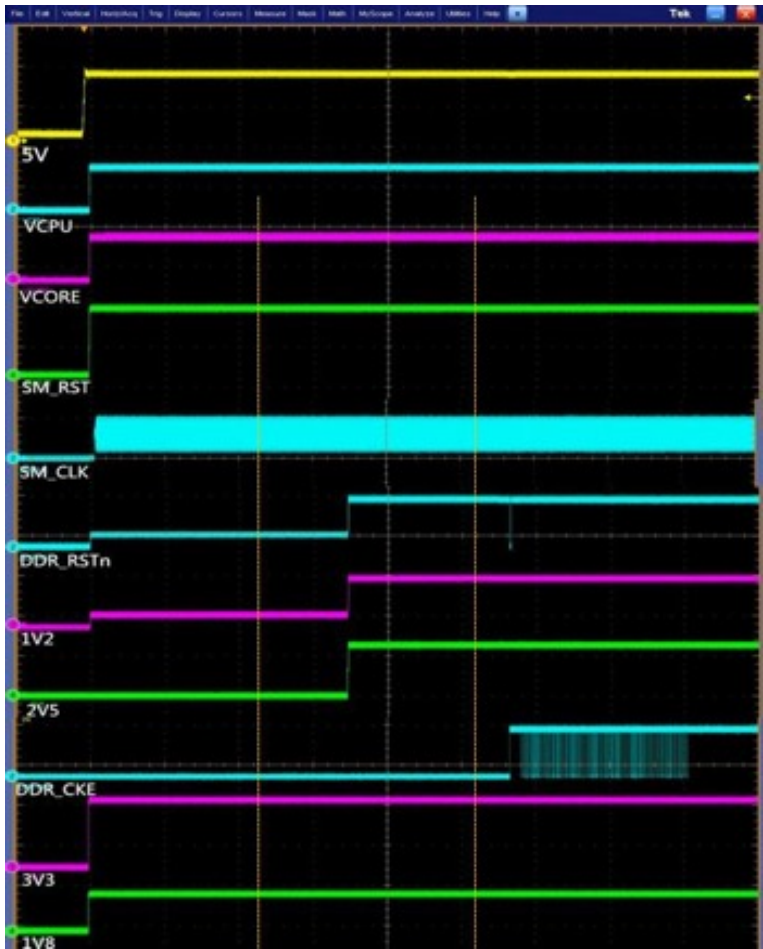
2. Test Condition

AC power: 220V@60Hz

DC power: 24V/5A

3. Power on specification

As SOC vendor Synaptic said that due to POR, do not care the timing. The sequence just follow as spec.



	1	2	3	4	5
PWR_3V3					
PWR_1V8					
		SM_RSTn			
			VCORE		
			VCPU		
				DDR_2V5	
					DDR_1V2

4. Power on Result and Picture

Test Item	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	0.4	Figure 1.	1	Pass
PWR_5V vs PWR_1V8	0.4	Figure 2.	1	Pass
PWR_5V vs PWR_DDR4_1V2	220	Figure 3.	5	Pass
PWR_5V vs SM_RSTIn	1.0	Figure 4.	2	Pass
PWR_5V vs PWR_CPU_1V05*	0.08	Figure 5.	1	Pass
PWR_5V vs PWR_CORE_1V05*	0.08	Figure 6.	1	Pass
PWR_3V3 vs PWR_DDR4_2V5	202	Figure 7.	4	Pass
PWR_3V3 vs PWR_VTT_0V6	202	Figure 8.	4	Pass

Note:

***: Ask Synaptic SOC vendor, they said the CPU and CORE are no timing limit. So the sequence is ok as currently setup.**

BFX-UA300 V015 DC Power sequence test

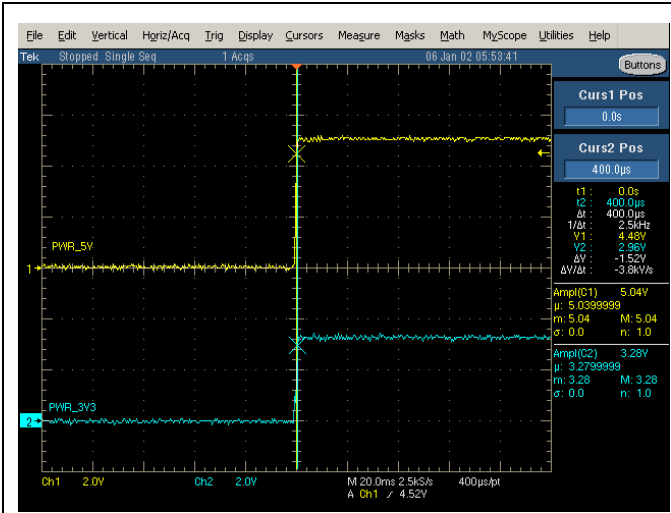


Fig. 1: PWR_5V vs PWR_3V3

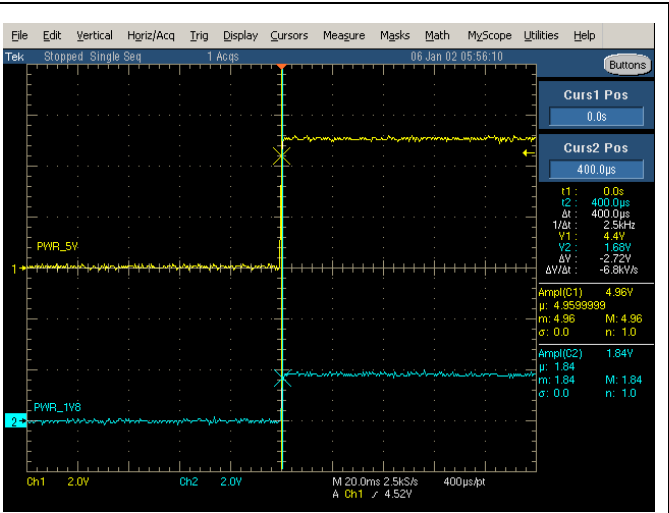


Fig. 2: PWR_5V vs PWR_1V8

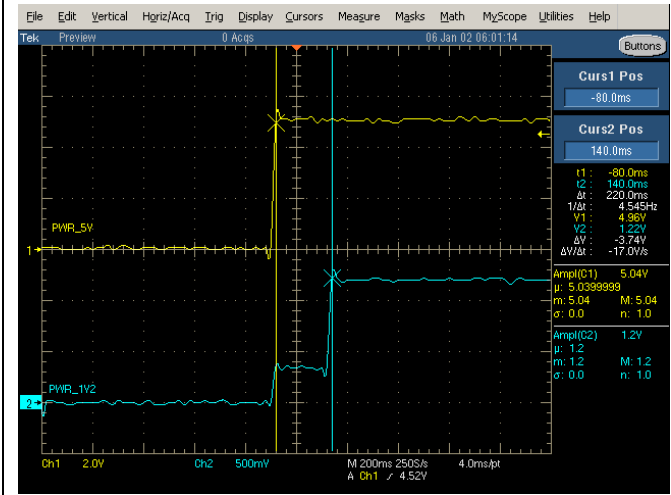


Fig. 3: PWR_5V vs PWR_DDR4_1V2

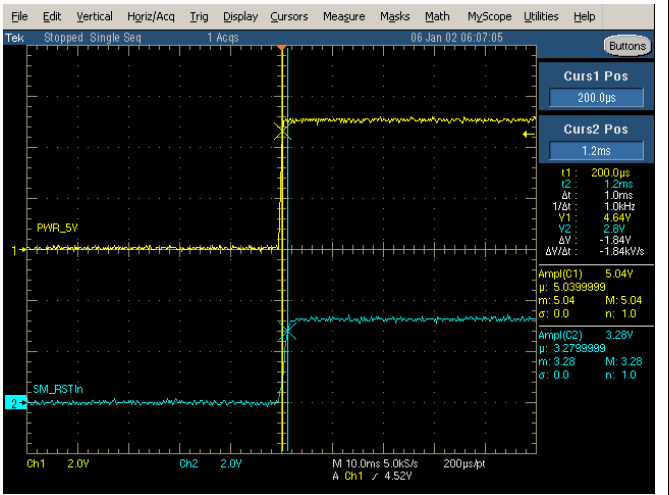


Fig. 4: PWR_5V vs SM_RSTIn

BFX-UA300 V015 DC Power sequence test

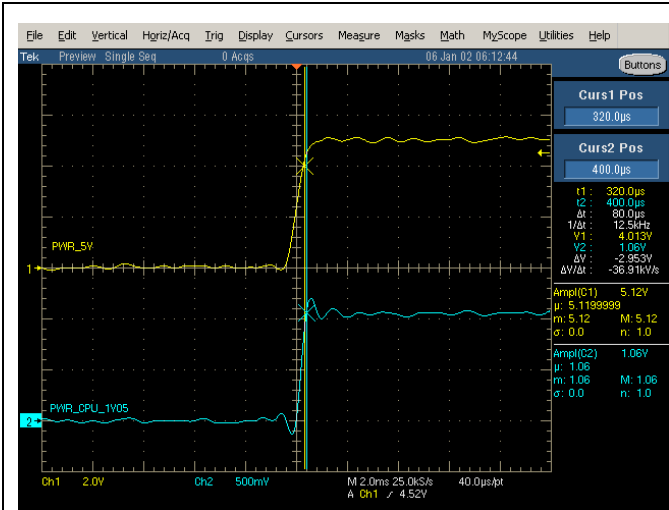


Fig. 5: PWR_5V vs PWR_CPU_1V05

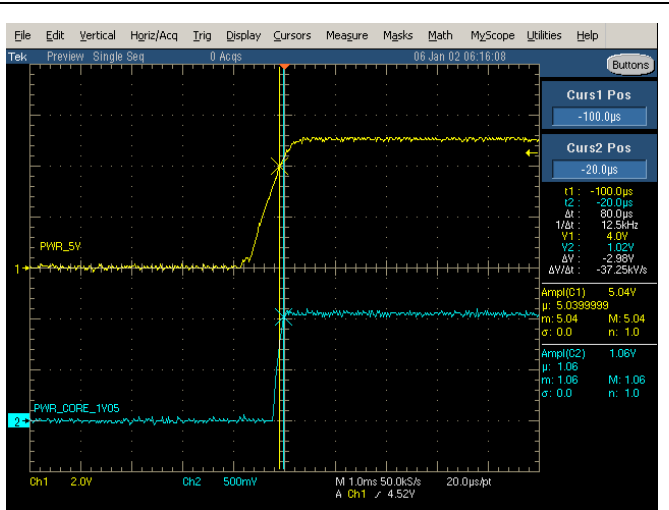


Fig. 6: PWR_5V vs PWR_CORE_1V05

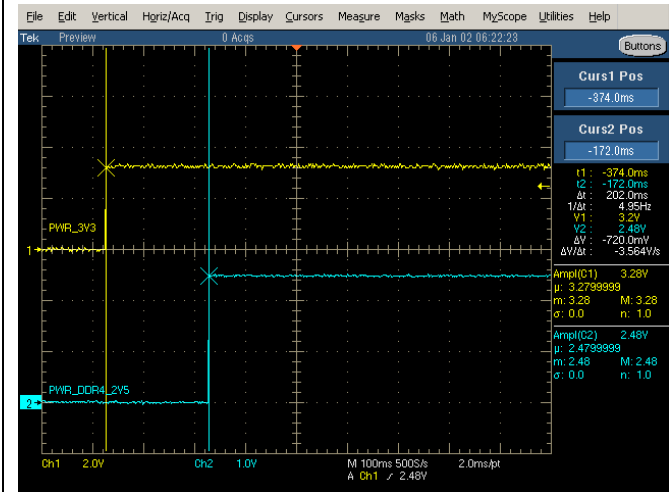


Fig. 7: PWR_3V3 vs PWR_DDR4_2V5

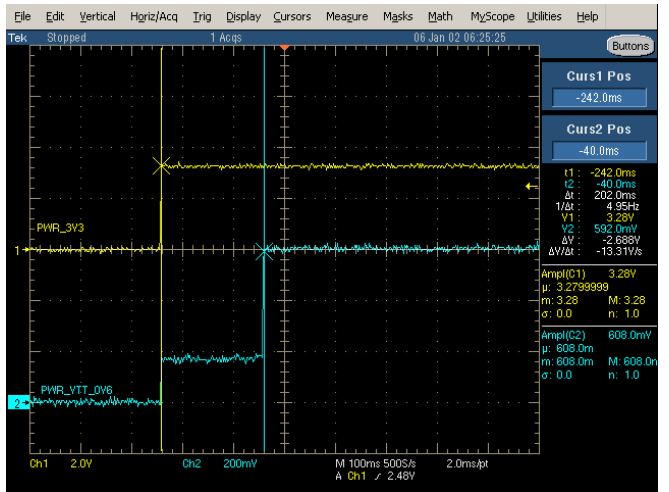


Fig. 8: PWR_3V3 vs PWR_VTT_0V6